The rough oxide **31** is typically formed by atmosphere chemical vapor deposition (APCVD) or sub-atmosphere CVD (SACVD) techniques, the deposition operation is under a mixture of ozone and Tetra-Ethyl-Ortho Silicate (TEOS) gases (O_3-TEOS), at a temperature range of 300° C. to 600° C., a pressure range of 300 to 760 Torr and a ozone concentration greater than 4%. This step is the key point of the present invention, the surface roughness of the rough oxide is a function of ozone concentration as shown in FIG. **8**. The rough oxides have ideal grain sizes which can serve as a proper etching mask when deposited in ozone concentration greater than 4% environment.

Referring now to FIG. **4**, by using rough oxide grains **31** as an etching mask, the thermal oxide **29**A in the isolation region and the silicon substrate **21** underneath are spontaneously etched to form multiple trenches which are about 2000 to 4000 Angstroms deep. The etching process is once again using dry etching with Cl_2, HBr and O_2 reactant gases. Alternatively, the trenches **33** are formed by two-step etching to etch the thermal oxide **29**A and the silicon substrate **21** separately.

Referring now to FIG. **5**, the rough oxide grains **31** and thermal oxide layer **29**A are removed. Then, filed oxidation is performed to form a smoother field oxide isolation **37** without bird's beak. Alternatively, the field oxide **37** may first grow, and then remove the rough oxide grains **31** and thermal oxide layer **29**A later. The local field oxide isolation regions without bird's beak according to the present invention is finally accomplished. Thereafter, the silicon substrate is ready for subsequent process steps.

The rough oxide grains **31** and thermal oxide layer **29**A are usually stripped by diluted hydrogen fluoride (HF) acid, but other types wet etching or dry etching may also work. The field oxidation is achieved by thermally oxide the silicon substrate **21** at a temperature range of about 900° C. to 1100° C. for about 60 to 150 minutes to obtain an ideal field oxide thickness.

Alternatively, FIGS. **2**, **5**, **6**, and **7** illustrate another preferred embodiment of the present invention. This embodiment proceed exactly as the proceeding embodiment up to the step of defining the active device and isolation regions.

Referring now to FIG. **6**, a very thin layer of second dielectric **30** which has a thickness of about 50 to 150 Angstroms is deposited over the entire silicon substrate **21** surface, followed by depositing a layer of rough oxide **31** with predetermined grain size overlaying the second dielectric layer **30** as shown in FIG. **6**.

The second dielectric layer **30** is typically using chemical vapor deposited oxide (CVD oxide) or the like, alternatively, fluoride doped silicate glass (FSG), phosphor us doped silicate glass (PSG), plasma enhanced CVD TEOS (PE-TEOS), low pressure CVD TEOS (LP-TEOS), nitride (Si_3N_4) or oxynitride (SiO_xN_y) can also be used.

Referring now to FIG. **7**, by using rough oxide grains **31** as an etching mask, the second dielectric layer **30**A and the silicon substrate **21** underneath are spontaneously etched to form multiple trenches **33** about 2000 to 4000 Angstroms deep in the isolation region. The etching process is once again using dry etching with Cl_2, HBr and O_2 reactant gases. Alternatively, the trenches **33** are formed by two-step etching to etch the second dielectric layer **30**A and the silicon substrate **21** separately.

Referring now to FIG. **5** once more, the rough oxide grains **31** and second dielectric layer **30**A are stripped. Then, filed oxidation is performed to form a smoother field oxide isolation **37** without bird's beak. Alternatively, the field oxide **37** may first grow, and then strip the rough oxide grains **31** and second dielectric layer **30**A later.

The field oxide isolation region formed according to the present invention has several advantages. First, the trenches provide deep oxide depth, and thereby high volume ratio and planar surface can be achieved. Besides, the enhanced trenches area also provides enough space for the silicon dioxide to expand, and results in smaller stress buildup and much less recessed bird's beak formation compared with the traditional LOCOS or STI processes.

While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the present invention.

What is claimed is:

1. A method of forming isolation region of an integrated circuit by means of rough oxide mask, comprising the steps of

(a) forming a first dielectric layer on a silicon substrate surface, and defining active device and isolation regions;

(b) growing a thermal oxide layer on the exposed said silicon substrate of the isolation region;

(c) forming a rough oxide layer over the entire silicon substrate surface;

(d) etching through said thermal oxide layer and silicon substrate to form multiple trenches in the isolation region by using said rough oxide as an etching mask; and

(e) removing said rough oxide and thermal oxide layers, and then oxidizing said silicon substrate within said trenches to form a field oxide isolation region.

2. The method according to claim **1**, wherein step (e) is first oxidizing said silicon substrate within said trenches to form a field oxide isolation region, and then removing said rough oxide and thermal oxide layers.

3. The method according to claim **1**, wherein said first dielectric layer is selecting from the group consisting of silicon dioxide, nitride and oxide/nitride double layers.

4. The method according to claim **1**, wherein said thermal oxide has a thickness of about 50 to 150 Angstroms.

5. The method according to claim **1**, wherein said rough oxide is composed of silicon dioxide formed with reactant gases of ozone and Tetra-Ethyl-Ortho Silicate (O3-TEOS).

6. The method according to claim **5**, wherein said O_3-TEOS is deposited in an environment with ozone concentration greater than 4%.

7. The method according to claim **5**, wherein said O_3-TEOS is deposited at a temperature range between 300° C. to 600° C.

8. The method according to claim **5**, wherein said O_3-TEOS is deposited at a pressure range between 300 to 760 Torr.

9. The method according to claim **5**, wherein said trenches are about 2000 to 4000 Angstroms deep.

10. A method of forming isolation region of an integrated circuit by means of rough oxide mask, comprising the steps of:

(a) forming a first dielectric layer on a silicon substrate surface, and defining active device and isolation regions;

(b) depositing a second dielectric layer over the entire silicon substrate surface; wherein said second dielectric layer is selected the group consisting of chemical vapor